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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/522,849	01/28/2005	Robert Kofler	AT02 0048 US	9368
65913	7590	10/30/2007		
NXP, B.V. NXP INTELLECTUAL PROPERTY DEPARTMENT M/S41-SJ 1109 MCKAY DRIVE SAN JOSE, CA 95131			EXAMINER BROWN, VERNAL U	
			ART UNIT 2612	PAPER NUMBER
			NOTIFICATION DATE 10/30/2007	DELIVERY MODE ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

<b>Office Action Summary</b>	<b>Application No.</b> 10/522,849	<b>Applicant(s)</b> KOFLER, ROBERT	
	<b>Examiner</b> Vernal U. Brown	<b>Art Unit</b> 2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☐ Responsive to communication(s) filed on 22 August 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 15-34 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 15-34 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) ✓                              | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### **DETAILED ACTION**

This action is responsive to communication filed on August 22, 2007.

#### ***Response to Amendment***

The examiner has acknowledged the cancellation of claims 1-14 and the addition of claims 15-34..

#### ***Response to Arguments***

Applicant's arguments with respect to claims 15-34 have been considered but are moot in view of the new ground(s) of rejection.

#### ***Claim Objections***

Claim 28-34 are objected to because of the following informalities: Claim 28 recites the limitation of "transmission means to receive" , transmission means is used for transmitting and not for receiving as claimed. The examiner suggests that the word "transmission" should be replace with "receiving". Appropriate correction is required.

#### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

Claims 15-20, 22, and 28-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Matsubara US Patent 5736728.

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Regarding claims 15 and 17, Matsubara teaches an integrated circuit comprising: circuit connecting contact (rectifying circuit) connected to the antenna transmission means of the transponder (col. 4 lines 61-67).

control means (81) for generating a voltage signal as a function of the operating mode of the transponder by generating a voltage, which is the minimum voltage, required to perform a write function (col. 9 lines 12-16);

a monitoring circuit comprising a comparator (82) to receive the control signal from the control means and a voltage based on the input voltage and generating a signalizing signal based on a relationship between a voltage threshold value and the voltage col. 9 lines 16-21).

Matsubara teaches a data processing circuit (36) to receive the signalizing signal from the monitoring circuit (col. 9 lines 21-30).

Regarding claim 16, Matsubara teaches a rectifier (32) to receive the input voltage and generate a voltage based on the input voltage (col. 4 lines 64-66).

Regarding claim 18, Matsubara teaches the monitoring circuit (82) comprises a reference voltage to receive a signal from the control means (81) and teaches generating voltage threshold values base on the control signal input from the control signal (col. 9 lines 12 -21).

Regarding claims 19-20, Matsubara teaches the data processing circuit recognizes read and write mode because it determines when a write operation is possible (col. 9 lines 22-30) and the 36 read the ID stores in the EEPROM when during a read operation (col. 1 lines 61-66).

Regarding claim 22, Matsubara teaches generating an interrupting signal to execute a finishing process of a write cycle (col. 11 lines 23-27) and this signal is considered a write signal.

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Regarding claim 28, Matsubara teaches a transponder comprising:  
receiving means (31) for receiving a control signal from communication station (col. 1 lines 50-60);  
circuit connecting contact (rectifying circuit) connected to the antenna transmission means of the transponder (col. 4 lines 61-67).

control means (81) for generating a voltage signal as a function of the operating mode of the transponder by generating a voltage, which is the minimum voltage, required to perform a write function (col. 9 lines 12-16);

a monitoring circuit comprising a comparator (82) to receive the control signal from the control means and a voltage based on the input voltage and generating a signalizing signal based on a relationship between a voltage threshold value and the voltage col. 9 lines 16-21).  
Matsubara teaches a data processing circuit (36) to receive the signalizing signal from the monitoring circuit (col. 9 lines 21-30).

Regarding claim 29, Matsubara teaches a rectifier (32) to receive the input voltage and generate a voltage based on the input voltage (col. 4 lines 64-66).

Regarding claim 30, Matsubara teaches monitoring circuit comprising a comparator (82) to compare the voltage threshold and to receive a signal from the control means (81) and teaches generating voltage threshold values base on the control signal input from the control signal (col. 9 lines 12 -21).

Regarding claim 31, Matsubara teaches the data processing circuit recognizes read and write mode because it determines when a write operation is possible (col. 9 lines 22-30) and the 36 read the ID stores in the EEPROM when during a read operation (col. 1 lines 61-66).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 21, 23-25, and 32-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsubara US Patent 5736728 in view of Liu US Patent Application Publication 20030162496.

Regarding claim 21, Matsubara teaches a reference voltage generating circuit for generating a threshold voltage (col. 11 lines 9-14) but is silent on teaching generating the threshold voltage from a plurality of preset. Liu in an analogous art teaches generating a threshold voltage value from a plurality of presets (paragraph 037).

It would have been obvious to one of ordinary skill in the art to modify the system of Matsubara as disclosed by Liu because the plurality of preset allows the reference voltage circuit to be adaptable and generate various threshold voltage value based on the application environment.

Regarding claim 23, Matsubara teaches a reference voltage generating circuit for generating a threshold voltage (col. 11 lines 9-14) but is silent on teaching generating the threshold voltage from a plurality of preset. Liu in an analogous art teaches generating a

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threshold voltage value from a plurality of presets (paragraph 037) but is silent on teaching the second voltage threshold value is higher than a first threshold value. The examiner take official notice that the threshold voltage determines by the preset is based on the voltage requirement of the circuitry and generating a second voltage threshold that is higher than the first voltage threshold is obvious to one of ordinary skill in the art.

It would have been obvious to one of ordinary skill in the art to modify the system of Matsubara as disclosed by Liu because the plurality of preset allows the reference voltage circuit to be adaptable and generate various threshold voltage value based on the application environment.

Regarding claim 24, Matsubara teaches a reference voltage generating circuit for generating a threshold voltage (col. 11 lines 9-14) but is silent on teaching generating the threshold voltage from a plurality of preset. Liu in an analogous art teaches generating a threshold voltage value from a plurality of presets stored in a configuration register (paragraph 037).

It would have been obvious to one of ordinary skill in the art to modify the system of Matsubara as disclosed by Liu because the plurality of preset allows the reference voltage circuit to be adaptable and generate various threshold voltage value based on the application environment.

Regarding claim 25, Matsubara teaches a reference voltage generating circuit for generating a threshold voltage (col. 11 lines 9-14) but is silent on teaching generating the threshold voltage from a plurality of preset. Liu in an analogous art teaches generating a

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threshold voltage value from a plurality of presets (paragraph 037) but is silent on teaching the second voltage threshold value is higher than a first threshold value. The examiner take official notice that the threshold voltage determines by the preset is based on the voltage requirement of the circuitry and generating a second voltage threshold that is higher than the first voltage threshold is obvious to one of ordinary skill in the art.

It would have been obvious to one of ordinary skill in the art to modify the system of Matsubara as disclosed by Liu because the plurality of preset allows the reference voltage circuit to be adaptable and generate various threshold voltage value based on the application environment.

Regarding claim 32, Matsubara teaches a reference voltage generating circuit for generating a threshold voltage (col. 11 lines 9-14) and recognizing read and write mode because it determines when a write operation is possible (col. 9 lines 22-30) and the 36 read the ID stores in the EEPROM when during a read operation (col. 1 lines 61-66) but is silent on teaching generating the threshold voltage from a plurality of preset. Liu in an analogous art teaches generating a threshold voltage value from a plurality of presets (paragraph 037) but is silent on teaching the first voltage threshold value is lower than a first threshold value. The examiner takes official notice that the threshold voltage determines by the preset is based on the voltage requirement of the circuitry and generating a second voltage threshold that is lower than the first voltage threshold is obvious to one of ordinary skill in the art.

It would have been obvious to one of ordinary skill in the art to modify the system of Matsubara as disclosed by Liu because the plurality of preset allows the reference voltage circuit



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to be adaptable and generate various threshold voltage value based on the application environment.

Regarding claim 33, Matsubara teaches a reference voltage generating circuit for generating a threshold voltage (col. 11 lines 9-14) and recognizing read and write mode because it determines when a write operation is possible (col. 9 lines 22-30) and the 36 read the ID stores in the EEPROM when during a read operation (col. 1 lines 61-66) but is silent on teaching generating the threshold voltage from a plurality of preset. Liu in an analogous art teaches generating a threshold voltage value from a plurality of presets (paragraph 037) but is silent on teaching the second voltage threshold value is higher than a first threshold value. The examiner take official notice that the threshold voltage determines by the preset is based on the voltage requirement of the circuitry and generating a second voltage threshold that is higher than the first voltage threshold is obvious to one of ordinary skill in the art.

It would have been obvious to one of ordinary skill in the art to modify the system of Matsubara as disclosed by Liu because the plurality of preset allows the reference voltage circuit to be adaptable and generate various threshold voltage value based on the application environment.

Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsubara US Patent 5736728 in view of Liu US Patent Application Publication 20030162496 and further in view of Gallagher, III et al. US Patent 6963270.

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Regarding claim 26, Matsubara is silent on teaching configuring a talk first mode in the transponder. Gallagher, III et al. in an analogous art teaches configuring a talk first mode in the transponder by transmitting a talk first command to the transponder (col. 7 lines 7-10).

It would have been obvious to one of ordinary skill in the art to configure the transponder of Matsubara in a talk first mode because this immediate communication of critical data from the transponder to the interrogator without requiring the interrogator to send a request to initiate a response from the transponder.

Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsubara US Patent 5736728 in view of Wuidart et al. US Patent 6650229.

Regarding claim 27, Matsubara teaches a processing circuit for processing the data from the reader (col. 9 lines 21-30) but is not explicit in teaching the data processing unit comprises a microprocessor. Wuidart et al. teaches the use of a microprocessor (17) to process data in the transponder and one skilled in the art recognizes that microprocessors are conventionally used in a transponder circuit.

It would have been obvious to one of ordinary skill in the art to modify the system of Matsubara as disclosed by Wuidart because a microprocessor provides the necessary processing power to process the data and generate control signal in a transponder.

Claim 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsubara US Patent 5736728 in view of Gallagher, III et al. US Patent 6963270.

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Regarding claim 34, Matsubara teaches the data processing circuit recognizes read and write mode because it determines when a write operation is possible (col. 9 lines 22-30) and the 36 read the ID stores in the EEPROM when during a read operation (col. 1 lines 61-66). Matsubara is silent on teaching configuring a talk first mode in the transponder. Gallagher, III et al. in an analogous art teaches a configuration register for storing control information, which corresponds to a transponder talk first mode of the transponder (col. 7 lines 41-47) and teaches storing various control information in the configuration register (col. 7 line 55 –col. 8 line 7). The examiner takes official notice that the voltage level of the generated is based on the voltage requirement of the circuitry and generating a third control signal that is lower than the first and second control is obvious to one of ordinary skill in the art.

It would have been obvious to one of ordinary skill in the art to configure the transponder of Matsubara in a talk first mode because this immediate communication of critical data from the transponder to the interrogator without requiring the interrogator to send a request to initiate a response from the transponder.

### ***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

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A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vernal U. Brown whose telephone number is 571-272-3060. The examiner can normally be reached on 8:30-7:00 Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Zimmerman can be reached on 571-272-3059. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.


Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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Vernal Brown  
October 22, 2007



BRIAN ZIMMERMAN  
PRIMARY EXAMINER